ADAPTIVE FILTER IMPLEMENTATION USING SWITCHED-CURRENT TECHNIQUE

Alexandre S. de la Vega

Universidade Federal Fluminense - TET/UFF
E-mail: delavega@telecom.uff.br

Antônio C. M. de Queiroz and Paulo S. R. Diniz

Universidade Federal do Rio de Janeiro - PEE/COPPE - EE/UFRJ
PoBox 68504, 21.945-970 - Rio de Janeiro - RJ - Brazil
E-mail: acmq@lps.ufrj.br, diniz@lps.ufrj.br

ABSTRACT

A CMOS switched-current adaptive filter architecture is presented. It is basically a finite impulse response (FIR) transversal filter adapted by using the Least-Mean-Square (LMS) adaptation algorithm. The design is based on delay and multiply-accumulator blocks. The implemented system can be switched to work either as an adaptive filter or as an FIR programmable filter. The adaptation signal can also be switched to allow for external control. Simulation results from a 4-tap FIR-LMS adaptive filter are also presented.

1. INTRODUCTION

Due to its simplicity and convergence characteristics [1], the least-mean-squares (LMS) algorithm is usually applied to the implementation of adaptive filters. Switched-current (SI) cells were proposed in [2], aiming to investigate their applicability on SI LMS-based adaptive filter implementation. Design constraints were analyzed in [3]. System slice simulations were presented in [4]. This work describes the implementation of the whole system. The main points addressed in the paper are as follows. Section 2 defines the system. The two basic system slices are presented in Sections 3 and 4. In Section 5, the complete implementation and some details are presented. Finally, simulation results are presented in Section 6.

2. IMPLEMENTED SYSTEM

A transversal finite impulse response (FIR) filter that uses the LMS adaptation algorithm is defined by the following equations

$$\boldsymbol{x}(k) = [x(k), x(k-1), \ldots, x(k-N)]^T$$

$$\boldsymbol{w}(k) = [w_0(k), w_1(k), \ldots, w_N(k)]^T$$

$$y(k) = \boldsymbol{w}^T(k)\boldsymbol{x}(k)$$

$$e(k) = d(k) - y(k)$$

$$\boldsymbol{w}(k+1) = \boldsymbol{w}(k) + 2\mu e(k)\boldsymbol{x}(k)$$

where $x(k)$ is the input signal, $\boldsymbol{w}(k)$ is the weight (coefficient) vector, $y(k)$ is the output signal, $d(k)$ is the reference signal and $e(k)$ is the error signal.

Due to the structure modularity two substructures were implemented: the filter-tap slice (FTS) and the feedback slice (FBS), both illustrated in Figs. 1 and 2.

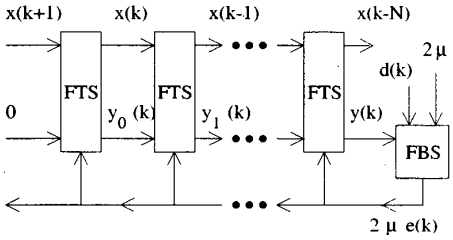

Figure 1: Implemented system.

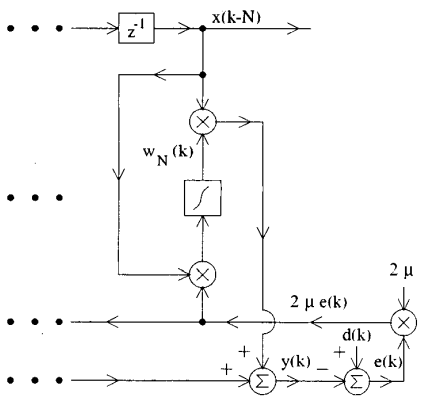

Figure 2: Original implementation.

Aiming to increase both the controllability as well as the observability of the system, the original structure has been modified. Including the switches shown in Fig. 3, the FIR coefficients can be programmed, the adaptation signal can be controlled or the system can adapt itself. Some signal taps were also added throughout the structure.

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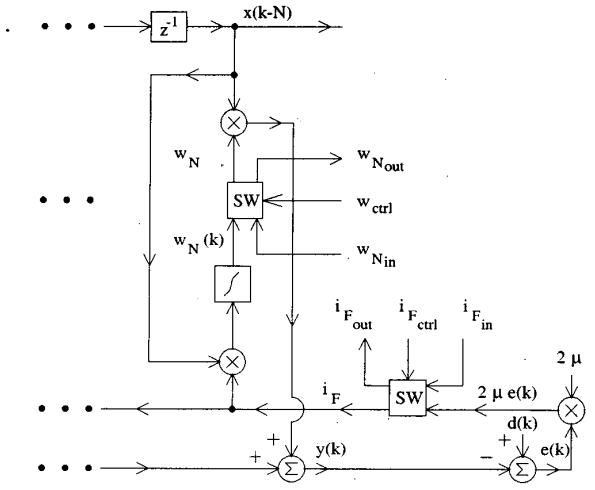

Figure 3: Modified implementation.

3. FILTER-TAP SLICE

The structure shown in Fig. 4 implements the filter-tap slice of the Fig. 3. The following cells were needed: unit delay, multiplier and integrator.

The unit delay comprises of two of the switched regulated cascode (SRC) memory cell (MC) illustrated in Fig. 5. Cascode current sources were used. Each memory cell has a signal tap. The first one is connected to an output pin, whilst the other one feeds the slice circuit.

Both the multiplier and the multiplier-integrator cells need copies (positive and negative) of its input signals. Cascode analogue inverters were used for that.

The multiplier MULT2 is built up from two current squarers, implementing the quarter-square technique [5].

The second multiplier and the integrator are added together into a single multiplier-difference-integrator cell, implemented by the selection switch set, the squarer and the two memory cells (MC), as proposed in [2], [3], [4].

The second selection switch set controls the slice coefficient source (internal or external). All the switches were implemented by means of transmission gates.

4. FEEDBACK SLICE

The feedback slice, shown in Fig. 6, calculates the adaptation signal ($2\mu e(k)$) from the FIR output ($y(k)$) and the two input signals ($d(k)$ and 2μ), as in Fig. 3.

In order to sample the reference signal ($d(k)$) and synchronize the feedback slice to the filter-tap slices, unit delays were employed. An additional memory cell was used to sink the input current whenever the unit delay is not sampling it.

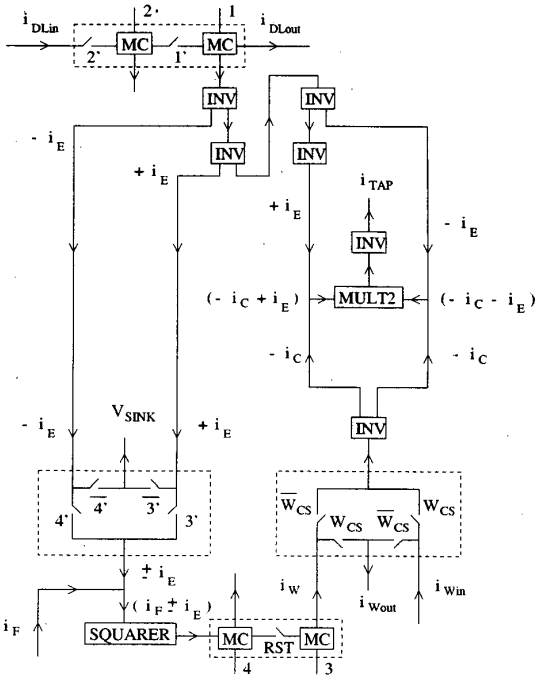

Figure 4: Filter-tap slice.

The multiplier is the same used in the filter-tap slice and needs copies (positive and negative) of its input signals. Here again cascode analogue inverters were used for that.

The selection switch set (transmission gates) controls the feedback current source (internal or external).

Finally, cascode analogue inverters supply copies of the adaptation signal for the filter-tap slices.

5. FINAL IMPLEMENTATION

The whole circuit for a 4-tap FIR-LMS adaptive filter can be seen in Fig. 7. It consists of: i) four filter-tap slices (upper four circuit lines), ii) one feedback slice (lower circuit line), iii) two bias circuits (top right), iv) a bank of seven digital inverters for control signal purposes (top left), and v) sixteen current-to-voltage converters [5] for the output signals (left, right and bottom).

The design was carried out under AMS 0.8μ CMOS technology. The layout is pad limited, needing 43 output pins and occupying an area of $1800 \times 1800(\mu m)^2$, approximately.

6. SIMULATION RESULTS

Simulation results are presented from two system configurations: an FIR filter and an adaptive filter.

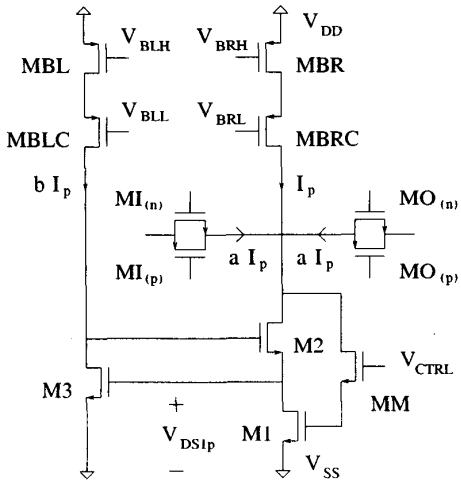

Figure 5: Memory cell structure.

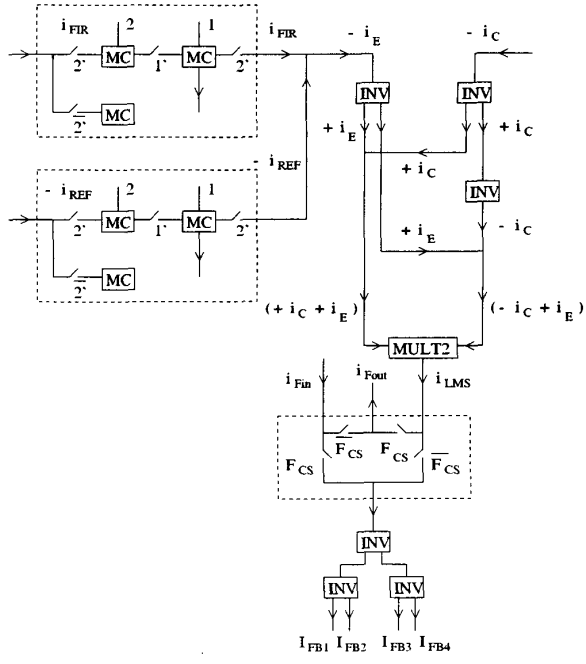

Figure 6: Feedback slice.

The clock sequence in Fig. 8 was used, starting with a reset arrangement, in order to have the correct initial conditions. From top to bottom, the first four signals are applied for the unit delay and the feedback slice memory cells $(1, 1', 2, 2')$. The fifth signal is the reset signal (RST). The last four signals are used by the multiplier-difference-integrator $(3, 3', 4, 4')$. During a sample-and-hold period of the multiplier-difference-integrator, the delay line is put on hold state and vice-versa. The sampling period was $T_{smp} = 9.2\mu s$.

The simulations were performed by using $V_{DD} = 5V$, $V_{SS} = 0V$ and $V_{ck} = 0 - 5V$. The memory cell in Fig. 5 was designed for a maximum input current of $40\mu A$, over bias currents of $I_p = 80\mu A$ and $bI_p = 8\mu A$. The squarer and the multiplier cells work under $I_{BiasSqr} = 40\mu A$. The total power consumption was less than $60mW$.

In the FIR simulation, the filter was driven with a pulse of $i_{pulse} = 20\mu A$. The filter coefficients were $I_{weight} =$ 10, 20, 20 and 10 μA.

The adaptive filter was fed with a convergence factor of $\mu = 20\mu A$, a sinewave reference signal of $d = 15\mu A \mid 15kHz$ and an input signal composed by four sinewaves of $x = (30 \mid 15), (1 \mid 15), (1 \mid 30)$ and $(1 \mid 45)$ $(\mu A \mid kHz)$.

The FIR filter response to a pulse can be seen in Fig. 9, while the adaptive filter error signal can be found in Fig. 10.

The Figs. 8, 9 and 10 were captured from the screen, on the simulation environment.

The effects of charge injection in the SRC memory cell matched those ones found in [6]. They are about $\Delta I = 0.1\mu A$ for a memory cell which has a settling time of $t_{st} = 20ns$, switched at $V_{ck} = 5V$ within $t_{rise/fall} = 5ns$.

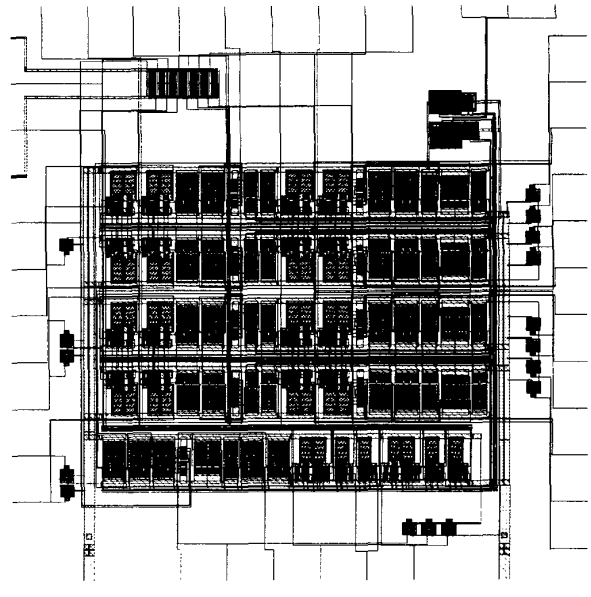

Figure 7: The 4-tap FIR-LMS adaptive filter layout.

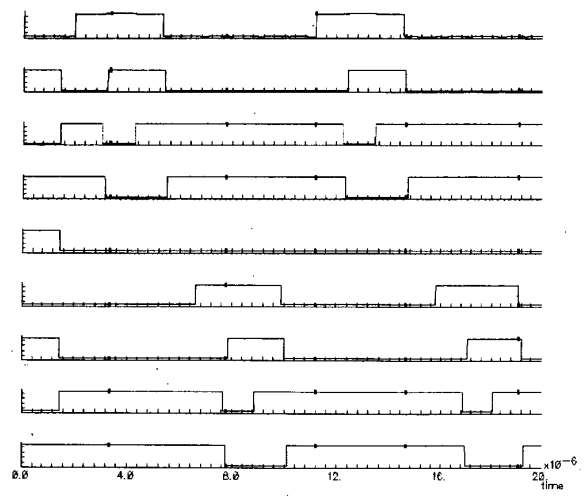

Figure 8: Clock sequence ($V \times \mu s$). See text for details.

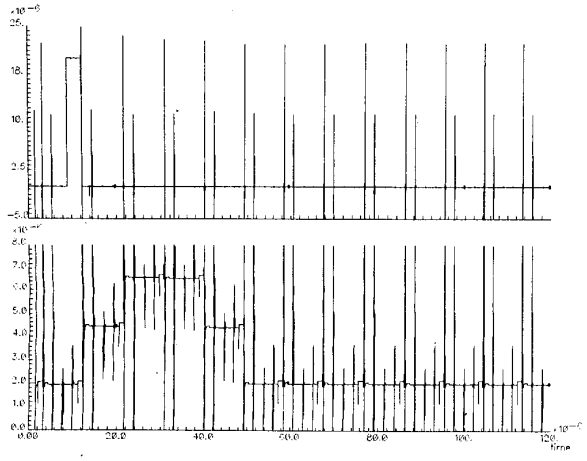

Figure 9: FIR input pulse $x(k+1)$ and output $y(k)$ ($\mu A \times \mu s$). See text for details.

7. CONCLUSION

Aiming an SI implementation for an LMS-based adaptive filter, some SI cells were presented previously. This work describes the final design of the whole system. The implemented system is configurable. It can work as an adaptive filter as well as an FIR filter. The adaptation signal can also be supplied from outside. Simulation results were presented, which show that the cells work as expected. Future work will investigate how to improve the performance of the cells and propose a more efficient system switching scheme.

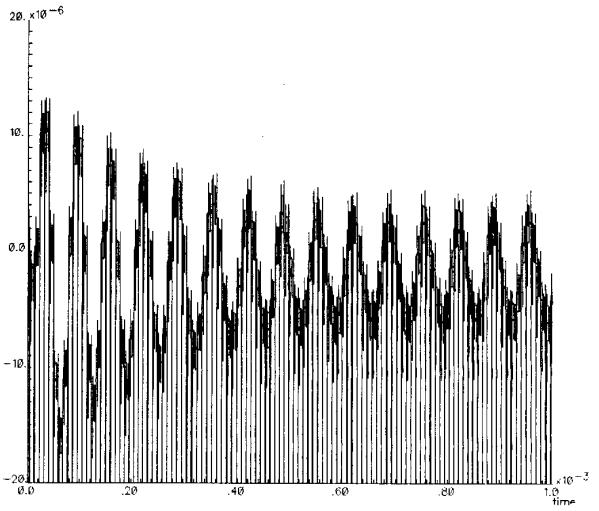

Figure 10: Adaptive filter error signal $e(k)$ ($\mu A \times \mu s$). See text for details.

8. REFERENCES

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